In the Specification:

Please delete the Paragraph beginning on Page 1, line 10 and replace the deleted Paragraph with the following Paragraph.

- -APPARATUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN A HOST PROCESSING AND A MULTI-TARGET DIGITAL SIGNAL PROCESSING IN AN ASYNCHRONOUS TRANSFER MODE; U.S. Patent Application No. ~~(Attorney Docket No. TI-33430)~~ 09/964,158; filed on even data herewith; invented by Martin Li, Jay Reimer, Shakuntala Anjanaiah, Natarajan Seshan, and Patrick Smith; and assigned to the assignee of the present application: APPARATUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN DATA PROCESSING UNITS IN THE ASYNCHRONOUS TRANSFER MODE AND IN THE I/O MODE; U.S. Patent Application No. ~~(Attorney Docket No. TI-33534)~~; 09/964,159; filed on even date herewith; invented by Shakuntala Anjanaiah, Roger Kyle Castille, and Natarajan Seshan; and assigned to the assignee of the present application: and APPARATUS AND METHOD FOR INPUT CLOCK SIGNAL DETECTION IN AN ASYNCHRONOUS TRANSFER MODE INTERFACE UNIT; U.S. Patent Application No. (~~Attorney Docket No. TI-33533)~~; 09/964,164; filed on even date herewith; invented by Shakuntala Anjanaiah; and assigned to the assignee of the present application are related applications.

Please delete the Paragraph beginning on Page 3, line 4 and replace this Paragraph with the following Paragraph.

- -A need has therefore been felt for apparatus and an associated method having the feature that an interface unit is provided that can transfer data using the UTOPIA protocol. It is another feature of the apparatus and associated method that the interface unit can be coupled to a direct memory access ~~management~~ unit of a processing unit acting in either a master or in a slave mode. It is a further feature of the apparatus and associated method to provide an interface unit that can operate in both a transmit mode or in a receive mode with the UTOPIA protocol. It is a still further feature of the present invention to provide for the buffering of data transferred in the UTOPIA protocol. It is yet another feature of the present invention that the interface unit can continuously transfer data cells. It is a more particular feature of the present invention to provide an interface unit responsive to a UTOPIA protocol having a buffer storage unit capable of storing two data cells. It is a still further particular feature of the apparatus and associated method that a buffer memory unit is provided for the receive mode and for the transmit mode.- -

Please delete the Paragraph beginning on page 3, Line 20 and replace this Paragraph with the following Paragraph.

- -The aforementioned and other features can be accomplished, according to the present invention, by providing a digital signal processor configuration with

an interface unit responsive to UTOPIA-defined signals. The UTOPIA interface unit is a generalized interface unit that provides the UTOPIA-defined signal set to external apparatus and responds to the UTOPIA-defined signal set from an external apparatus. The interface unit exchanges signals between the direct memory access unit of the data processing unit, of which the interface unit is a component, and a communication bus. The signals exchanged between the interface unit and the communication bus are implemented to provide efficient transfer of data there between. In particular, the interface unit can exchange data cells continuously with a communication bus. The interface unit includes a processor (acting as a state machine) for receiving and generating signals and buffer memory unit for buffering the flow data. The interface unit can operate in a master state with both a transmit mode and a receive mode and can operate in a slave state in both a transmit and receive mode.- -

Please delete the Paragraph beginning a page 5, line 13 and replace this Paragraph with the following Paragraph.

- -Figure 10A illustrates the asynchronous transfer mode Utopia protocol signals with a master-state data processing unit in a transmit mode and a plurality of slave-state data processing units in a receive mode, while Figure 10B illustrates the asynchronous transfer mode Utopia protocol signals with a master-state data

processing unit ~~is~~ in a receive mode and a plurality of slave-state data processing units in a transmit mode.- -

Please delete the Paragraph beginning on Page 9, line 26 and replace this Paragraph with the following Paragraph.

- -Referring to Fig. 5, a timing diagram illustrating the relationship of the signals for the asynchronous transfer mode interface unit **14** in the receive-mode depicted in Fig. 4 ~~are~~ is shown. The signals are synchronized by the URCLK signal. The master processor applies the ADDR {4:0} signal group to the slave processors. The identified slave processor responds to the ADDR {4:0} signal with the appropriate CLAV signal. When an active CLAV signal is applied, the ADDR {4:0} signals are reapplied along with the ENB signal. The slave starts receiving data along with an SOC signal. The DATA {15:0} signals continue to be received until the cell has been completely transferred.- -

Please delete the paragraph beginning on Page 10, Line 4 and replace this Paragraph with the following Paragraph.

- -Referring to Fig. 6, the signals exchanged by the interface unit **18** in the master-transmit mode ~~is~~ are shown. The processor **184** of the interface unit **18** receives the UXCLK signal and the UXCLAV signal. The

interface unit **184** applies the UXADDR [4:0] signals, the UXENB signal, the UXSOC signal, and the UXDATA {15:0} signals to the slave processing unit. The processor **184** applies the WD_RD signal to the buffer memory unit **182** and processor **184** receives the DATA {31:0} signals and the CLAV signals from the buffer memory unit **182**. The buffer memory unit **182** applies the EVENT signal to the direct memory access unit **14** and the buffer memory unit **182** receives the DATA {31:0} signals, the ADDR {31:0} signals, and the WD_WR signal from the direct memory access unit **14**. In the master-state transmit state the DATA signals are transmitted from the direct memory access unit **14** to the buffer out memory unit **182**, and then through the processor **184** to the external component. The WD_WR signal permits the DATA signals to be transmitted from the direct memory access unit **14** to the buffer memory unit **182**. The CLAV signal and the WR_RD signal permit the DATA signals to be transferred from the buffer memory unit **182** to the processor **184** and, subsequently to the external component.- -

Please delete the Paragraph beginning on Page 11, Line 23 and replace this Paragraph with the following Paragraph.

- -Referring to Fig. 10A and Fig. 10B, a data processing system is shown having a master-state data processing unit **91** and a plurality of slave-state data processing units **92A** through **92N**. In Fig. 10A, the master-state data processing unit **91** is in a transmit mode, while the slave-state data processing units **92A**

through **92N** are in a receive mode. In Fig. 10B, the master-state data processing unit **91** is in a receive mode while the slave-state data processing units **92A** through **92N** are in a transmit mode. In Fig. 10A, the master data processing unit **91** (in the transmit mode) generates the UXCLK, the UXADDR, the UXENB, the UXSOC, and the UXDATA signals become the URCLK, the URADDR, the URENB, the URSOC, and the URDATA signals, respectively, when applied to the slave data processing units **92A-92N** (in the receive mode). The URCLAV signals from the slave data processing units **92A-92N** are applied to the master data processing unit **91** as the UXCLAV signal. In Fig. 10B, the master data processing unit **91** (in the receive mode) generates the URCLK, the URADDR, and the URENB signals that are applied to the slave data processing units **92A-92N** (in the transmit mode as the UXCLK, the UXADDR, and UXENB signal respectively). The slave data processing units **92A-92N** generate the UXCLAV, the UXSOC, and the UXDATA signals that are applied to the master data processing unit **91** as the URCLAV, the URSOC, and the URDATA signals, respectively.- -

Please delete the Paragraph beginning on Page 12, line 28 and replace this Paragraph with the following Paragraph.

- -Referring to Fig. 12, the contents of the interface control register according to the preferred embodiment ~~is~~ are shown. In the UREN/UXEN fields, a logic "0" indicates that the receive/transmit port is disabled, while a logic "1" indicates that the interface

receive port is enabled. This designation is true in both the master and the slave modes. In the URMSTR/UXMSTR fields, a logic "0" indicates that the interface unit is operating in a slave (default) mode, while a logic "1" indicates that the interface unit is operating in a master mode. In the RUDC/XUDC fields, a user defined (i.e., standard or extended) data cell is specified for both the receive and the transmit operational modes. This field is used in the slave mode. In the SLID/SLEND field, this field identifies the address of the coupled processor unit in the slave mode. In the master mode, this field identifies the last of the processors coupled to the interface unit. In the UPM field, this field identifies whether a polling takes place in a round-robin manner or from a fixed address. The U16M field determines whether data transfers are 8 bits or 16 bits for both the input and the output interfaces. The MPHY field determines whether the interface unit is coupled to a single processor (logic "0") or to multiple processors. The ULB field determines whether the interface unit is in a loop-back mode. In the loop-back mode (i.e., logic "1"), the receive and transmit sections are coupled and the master is determined by the URMSTR/UXMSTR fields. The BEND field determines the data transfer in a big endian or little endian format.- -

Please delete the Paragraph beginning on Page 13, Line 17 and replace this Paragraph with the following Paragraph.

Referring to Fig. 13, the operation of the (transmit) EVENT signal is illustrated. After initialization of the transmit portion of the UTOPIA interface unit in step 1300 or as part of the continuing operation of the interface unit, a determination is made in step 1301 whether a space for the storage of a complete data cell is available in the transmit buffer memory unit. When the determination is yes, then ~~is~~ in step 1302 a transmit EVENT signal is applied to the direct memory access unit. In response to the generation of the EVENT signal, a data cell is transmitted through the direct memory access unit to the transmit buffer memory storage unit in step 1303. In step 1304, as soon as the transfer of the data cell has begun and the first word of the cell is written, the EVENT signal is cleared. Note that the EVENT signal is reasserted as soon as the first word is written and the buffer memory unit has space available. The immediate reassertion of the EVENT signal improves the interface unit throughput. The process than ~~returned~~ returns to step 1301 to determine whether space in the transmit buffer memory unit is available for storage of an entire data cell. When the determination is step 1301 is negative, the process returns to step 1301 and continues to cycle until space is available for the storage of an entire data cell.

Please delete the Paragraph beginning on Page 14, Line 30 and replace this Paragraph with the following Paragraph.

The foregoing description has described the interface unit as including a buffer memory unit. In the preferred embodiment, the buffer memory unit is implemented by a first-in/first out memory unit. The memory unit is provided with the capacity to store two data cells. The communication bus causes the signals to be exchanged between the master unit and the slave unit to have a relatively slow clock speed. Because of the relatively slow clock speed of the communication bus, the filling or emptying of the buffer memory in the direction of the communication will be much slower than the filling and the emptying of the buffer memory unit in the direction of the direct access memory unit. Similarly, although the direct memory access unit can handle only one data transfer at a time, because of the difference in clock speed between the communication bus and the processing unit of which the direct memory access unit is a part, the configuration does not limit transfer of data.